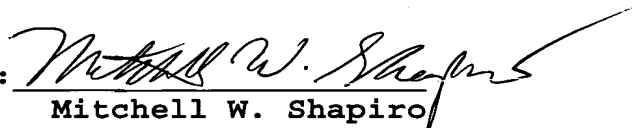


this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been requested separately, such extension is hereby requested.

Respectfully submitted,

MWS:lmb

By:



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December 17, 2001

10009826 . 031902

Marked-Up Copy of Claims -- PCT/JP00/03723

1. (Amended) A semiconductor memory device  
comprising:

a semiconductor substrate;

a memory cell array, disposed on the semiconductor  
substrate, having plural memory cells, word lines and data  
lines for selecting the memory cells; and

a peripheral circuit disposed on the semiconductor  
substrate;

wherein the memory cell has a multi-layer of a  
conductive layer, an insulating layer and plural  
semiconductor layers containing impurities of different  
conduction type, and a potential can be applied to the  
insulating layer that enables the movement of carriers by  
way of the multi-layer.

8. (Amended) A semiconductor memory device as  
defined in [any one of claims 4 to 7] claim 4, wherein an  
impurity concentration of the layer present in contact with  
the surface of the semiconductor substrate among the plural  
semiconductor layers containing impurities for forming the  
memory cell is

$1 \times 10^{17} \text{ cm}^{-3}$  or less on the surface of the semiconductor  
substrate.

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30. (Amended) A semiconductor memory device as  
defined in claim 1, wherein at least a portion of a memory  
device is disposed in the semiconductor substrate and a  
memory capacity is 256 Mbits or more.

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